CLAIMS

What is claimed is:

1. A method of manufacturing a double-gate integrated circuit comprising:

forming a laminated structure having a channel layer and first insulating layers on each side of said channel layer;

forming openings in said laminated structure;

forming drain and source regions in said openings;

doping said drain and source regions, using said openings in said laminated structure to align said doping;

removing portions of said laminated structure to leave said channel layer suspended from said drain and source regions;

forming a second insulating layer to cover said drain and source regions and said channel layer; and

forming a double-gate conductor over said second insulating layer such that said double-gate conductor includes a first conductor on a first side of said channel layer and a second conductor on a second side of said channel layer.

2. The method in claim 1, wherein, during said forming of said double-gate conductor, said drain and source regions and said second insulating layer self-align said double-gate conductor.

3. The method in claim 1, wherein said forming of said laminated structure includes forming a bottom insulator layer adjacent one of said first insulating layers and said method further comprises, after said forming of said double-gate conductor, forming a top insulator layer on an opposite side of said double-gate conductor from said bottom insulator layer, such that a thickness of said second insulating layer is independent of a thickness of said bottom insulator layer and said top insulator layer.

4. The method in claim 1, wherein said forming of said drain and source regions comprises epitaxially growing drain and source regions in said openings from said channel layer.

5. The method in claim 4, wherein said epitaxially growing of said drain and source regions includes introducing one or more of Si, Ge, C, N and an alloy.

6. The method in claim 1, wherein said forming of said drain and source regions comprises epitaxially growing a portion of said drain and source regions in said openings from said channel layer and filling a remainder of said openings with amorphous silicon to complete said drain and source regions.

7. The method in claim 1, wherein:

said forming of said laminated structure includes attaching a substrate to said laminated structure;

said forming of said openings includes exposing said substrate; and

said forming of said drain and source regions comprises epitaxially growing said drain and source regions in said openings from said channel layer and said substrate.

8. The method in claim 1, wherein said channel layer comprises a single crystal silicon layer and said forming of said laminated structure includes depositing said first insulating layers on each side of said single crystal silicon wafer.

9. The method in claim 1, wherein, before said forming of said drain and source regions, said method further comprises forming spacers in said openings.

10. A method of manufacturing a double-gate metal oxide semiconductor transistor comprising:

forming a laminated structure having a single crystal silicon channel layer and insulating oxide and nitride layers on each side of said single crystal silicon channel;

forming openings in said laminated structure;

forming drain and source regions in said openings;

doping said drain and source regions, using said openings in said laminated structure to align said doping;

removing portions of said laminated structure to leave said single crystal silicon channel layer suspended from said drain and source regions;

forming an oxide layer to cover said drain and source regions and said single crystal silicon channel layer; and

forming a double-gate conductor over said oxide layer such that said double-gate conductor includes a first conductor on a first side of said single crystal silicon channel layer and a second conductor on a second side of said single crystal silicon channel layer.

11. The method in claim 10, wherein, during said forming of said double-gate conductor, said drain and source regions and said oxide layer self-align said double-gate conductor.

12. The method in claim 10, wherein said forming of said laminated structure includes forming a lower oxide layer adjacent one of said first insulating layers and said method further comprises, after said forming of said double-gate conductor, forming an upper oxide layer on an opposite side of said double-gate conductor from said lower oxide layer, such that a thickness of said gate oxide layer is independent of a thickness of said upper oxide layer and said lower oxide layer.

13. The method in claim 10, wherein said forming of said drain and source regions comprises epitaxially growing silicon in said openings from said single crystal silicon channel layer.

14. The method in claim 13, wherein said epitaxially growing of said silicon includes introducing one or more of Si, Ge, C, N and an alloy.

15. The method in claim 10, wherein said forming of said drain and source regions comprises epitaxially growing silicon in a portion of said openings from said single crystal silicon channel layer and filling a remainder of said openings with amorphous silicon to complete said drain and source regions.

16. The method in claim 10, wherein:

said forming of said laminated structure includes attaching a silicon substrate to said laminated structure;

said forming of said openings includes exposing said silicon substrate; and

said forming of said drain and source regions comprises epitaxially growing silicon in said openings from said single crystal silicon channel layer and said silicon substrate.

17. The method in claim 10, wherein, before said forming of said drain and

source regions, said method further comprises forming spacers in said openings.

Sub B1

18. A double-gate integrated circuit comprising:

a channel layer;

doped drain and source regions connected to said channel layer;

a gate insulating layer covering said channel layer and said doped drain and source regions;

a double-gate conductor over said insulating layer, said double-gate conductor including a first conductor on a first side of said channel layer and a second conductor on a second side of said channel layer;

an upper insulator layer adjacent on a first side of said double-gate conductor; and

a lower insulator layer on an opposite side of said double-gate conductor from said upper insulator layer, wherein a thickness of said gate insulating layer is independent of a thickness of said upper insulator layer and said lower insulator layer.

19. The double-gate integrated circuit in claim 18, wherein, said first conductor and said second conductor are self-aligned by said doped regions and said gate insulating layer.

20. The double-gate integrated circuit in claim 18, wherein said doped drain

and source regions comprise silicon epitaxially grown from said channel layer.

21. The double-gate integrated circuit in claim 20, wherein said epitaxially grown silicon includes one or more of Si, Ge, C, N and an alloy.

sub B2

22. The double-gate integrated circuit in claim 18, wherein said drain and source regions comprise amorphous silicon and silicon epitaxially grown from said channel layer.

23. The double-gate integrated circuit in claim 18, further comprising a substrate connected to said lower insulator layer, wherein said drain and source regions comprise silicon epitaxially grown from said channel layer and from said substrate.

24. The double-gate integrated circuit in claim 18, wherein said channel layer comprises a single crystal silicon layer.

add B3